AMENDMENTS TO THE CLAIMS

Please amend claims 1, 4, 7-11, 14, 16, 18, and 22. No new claims are presented in this paper, nor have any claims been canceled in this paper. The following listing of the claims replaces all previous listings.

1. **(Currently Amended)** A system for determining a jitter tolerance of an optoelectronic device, comprising:

a generation circuit configured to generate a first sequence of bits and to transmit said first sequence of bits to a delay circuit configured to individually transmit each of said bits in said first sequence of bits to said opto-electronic device, each bit of said first sequence of bits subject to a delay prior to being transmitted to said opto-electronic device; and

comparison circuitry configured to receive a second sequence of bits from said optoelectronic device, said second sequence of bits being derived by said opto-electronic device from said first sequence of bits;

wherein said comparison circuitry compares said second sequence of bits to said first sequence of bits and wherein said jitter tolerance of said opto-electronic device is determined by reference to said comparison.

2. **(Original)** The system of claim 1, wherein said delay is changed by a predefined amount at a predefined frequency.

3. **(Original)** The system of claim 1, wherein said delay is changed by a plurality of predefined amounts at a plurality of predefined frequencies.

4.   **(Currently Amended)**   The system of claim 1, wherein ~~the~~ said optoelectronic device is a transceiver.

5.   **(Original)**   The system of claim 1, wherein said generation circuit includes a bit sequence generator and a serializer/deserializer.

6.   **(Original)**   The system of claim 1, wherein said comparison circuitry includes a controller that receives said first and second sequences of bits and compares said sequences to determine a number of bit errors, and wherein said number of bit errors is used to determine said jitter tolerance.

7.   **(Currently Amended)**   In a system for measuring a jitter tolerance of an optoelectronic device, said system being adapted to electrically communicate with ~~the~~ said optoelectronic device and at least one master device, said system comprising a first bit sequence generator, a second bit sequence generator, a delay circuit, and a controller, a method for computing ~~the~~ said jitter tolerance comprising the steps of:

generating a first sequence of bits and transmitting said first sequence of bits to ~~the~~ said delay circuit;

delaying said first sequence of bits and individually transmitting each bit in said first sequence of bits to ~~the~~ said optoelectronic device;

transmitting a second sequence of bits from ~~the~~ said optoelectronic device to ~~the~~ said controller, said second sequence of bits derived by ~~the~~ said optoelectronic device from ~~the~~ said first sequence of bits;

comparing said first sequence of bits to said second sequence of bits to calculate a bit error rate; and

using said bit error rate to determine said jitter tolerance.

8.   **(Currently Amended)**   The method of claim 7, wherein said delaying step includes delaying said <u>first sequence of</u> bits by a predefined amount at a predefined frequency.

9.   **(Currently Amended)**   The method of claim 7, wherein said delaying step includes delaying said <u>first sequence of</u> bits by a plurality of predefined amounts at a plurality of predefined frequencies.

10.   **(Currently Amended)**   The method of claim 7, wherein ~~the~~ <u>said</u> optoelectronic device is a transceiver.

11.   **(Currently Amended)**   A system for determining a signal attenuation tolerance of an optoelectronic device, comprising:

a generation circuit configured to generate a first sequence of bits and to transmit said first sequence of bits to a delay circuit configured to <u>delay said first sequence of bits and to then</u> individually transmit <u>each</u> ~~bits~~ in said first sequence <u>of bits</u> to an attenuator configured to perform an attenuation of a power level of said first sequence of bits by a predefined amount and to then transmit said first sequence of bits to ~~the~~ <u>said</u> optoelectronic device; and

comparison circuitry configured to receive a second sequence of bits from ~~the~~ <u>said</u> optoelectronic device, said second sequence of bits being derived by ~~the~~ <u>said</u> optoelectronic device from said first sequence of bits;

wherein said comparison circuitry compares said second sequence of bits to said first sequence of bits and wherein said signal attenuation tolerance of said optoelectronic device is determined by reference to said comparison.

12. **(Original)** The system of claim 11, wherein said comparison circuitry includes a controller that receives said first and second sequences of bits and compares said sequences to determine a number of bit errors, and wherein said number of bit errors is used to determine said attenuation tolerance.

13. **(Original)** The system of claim 12, wherein said delay is changed by a predefined amount at a predefined frequency.

14. **(Currently Amended)** The system of claim 13, wherein said attenuator is configured to attenuate said power level at a plurality of attenuation levels, and wherein, for each attenuation level, said delay is changed by said predefined amount at said predefined frequency, and said a bit error rate is calculated for each of said attenuation levels, said bit error rates being combined to determine said attenuation tolerance.

15. **(Original)** The system of claim 12, wherein said delay is changed by a plurality of predefined amounts at a plurality of predefined frequencies.

16. **(Currently Amended)** The system of claim 15, wherein said attenuator is configured to attenuate said power level at a plurality of attenuation levels, and wherein, for each attenuation level, said delay is changed by each of said predefined amounts at each of said predefined frequencies to form a plurality of data points, and said a bit error rate is calculated for each data point of said plurality of data points, said bit error rates for each data point of said plurality of data points being combined to determine said attenuation tolerance.

17. **(Original)** The system of claim 11, wherein said optoelectronic device is a transceiver.

18. **(Currently Amended)** In a system for measuring an attenuation tolerance of an optoelectronic device, said system being adapted to electrically communicate with ~~the~~ said optoelectronic device and an optical attenuator, said system comprising a first bit sequence generator, a second bit sequence generator, a delay <u>circuit</u>, and a controller, a method for computing ~~the~~ <u>said</u> attenuation tolerance comprising the steps of:

generating a first sequence of bits and transmitting said first sequence of bits to ~~the~~ <u>said</u> delay <u>circuit</u>;

delaying said first sequence of bits and individually transmitting said <u>first sequence of</u> bits to ~~the~~ <u>said</u> optoelectronic device;

transmitting a second sequence of bits from ~~the~~ <u>said</u> optoelectronic device to ~~the~~ <u>said</u> optical attenuator, said second sequence of bits derived by ~~the~~ <u>said</u> optoelectronic device from ~~the~~ <u>said</u> first sequence of bits;

attenuating a power level of said second sequence of bits and transmitting said first sequence of bits and said second sequence of bits to ~~the~~ <u>said</u> controller;

comparing said first sequence of bits to said second sequence of bits to calculate a bit error rate; and

using said bit error rate to determine said attenuation tolerance.

19. **(Original)** The method of claim 18, wherein said delaying step includes delaying said first sequence of bits by a predefined amount at a predefined frequency.

20. **(Original)** The method of claim 19, wherein said attenuating step includes attenuating said power level at a plurality of attenuation levels, and wherein, for each attenuation level, said delay is changed by said predefined amount at said predefined frequency, and said bit error rate is calculated for each of said attenuation levels, said bit error rates being combined to determine said attenuation tolerance.

21.   **(Original)**   The method of claim 18, wherein said delaying step includes delaying said first sequence of bits by a plurality of predefined amounts at a plurality of predefined frequencies.

22.   **(Currently Amended)**   The method of claim 21, wherein said attenuating step includes attenuating said power level at a plurality of attenuation levels, and wherein, for each attenuation level, said delay is changed by each of said predefined amounts at each of said predefined frequencies to form a plurality of data points, and said bit error rate is calculated for each <u>data point</u> of said plurality of data points, said bit error rates for each <u>data point</u> of said plurality of data points being combined to determine said attenuation tolerance.